AMENDMENTS TO THE ABSTRACT

Please add the following paragraph for the abstract:

Method for fabricating a semiconductor memory element arrangement. A layer system, including a floating gate and a tunnel barrier arrangement formed on the floating gate, is formed on an electrically insulating layer. A first trench structure is formed in the layer system, and the first trench structure has first parallel trenches extending as far as the insulating layer. A second trench structure is formed in the layer system, and has second parallel trenches arranged perpendicular to the first trenches and extending as far as the insulating layer. First and second gate electrodes are formed in the first and second trench structures. The first gate electrode is adjacent to the floating gate through which first gate electrode electrical charge can be fed or can be dissipated from. The second gate electrode is adjacent to the tunnel barrier arrangement, and can control an electrical charge transmission of the tunnel barrier arrangement.